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Electronic Tuning Square-Wave Generators with Improved Linearity Using Operational Transresistance Amplifier

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Abstract: The following study introduces two brand-new electronic tunable current-mode square-wave generators. Two NMOS depletion mode transistors, one operational trans-resistance amplifier (OTRA), and two passive components are all included in the first suggested square-wave generator circuit. A square wave with almost equal and fixed duty cycles is produced by this circuit. The second suggested design uses two passive components, two NMOS depletion mode transistors, and two linked diodes to enable independent control of the on-duty and off-duty cycles. The passive components attached to the circuit allow the suggested circuits to change their frequency. Moreover, the suggested circuits can also be used for electronic tuning. The measured results that are included in the paper show the linear variation of a time period as compared with existing OTRA based square waveform generator. The performance of the proposed circuits is examined while using SPICE models. These circuits are built on a laboratory breadboard using commercially available Current Feedback Operational Amplifier (AD844 AN) and passive components are connected externally and tested for square waveform generation. The obtained results demonstrate good agreement with the theoretical values.

Keywords: waveform generators; operational transresistance amplifier; analog integrated circuit design; current mode waveform generators

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1. Introduction

The square-wave generator is widely operated in many electronic fields, such as digital, instrumentation, and communication systems. Conventionally, Operational Amplifier (Op-Amp) is used to generate square waveform along with some passive components. These voltage-mode (Op-Amp) circuits pose some drawbacks, such as complex internal circuitry, lower slew rate, constant gain bandwidth product, and more passive components are, however, required to generate the waveforms [1].

Recently, an alternative approach, called current-mode technology, has attracted considerable attention for analog circuit designers, due to its advantage over voltage-mode devices, like high performance, high linearity, wide dynamic range, low power consumption, simple circuitry, and versatility over voltage-mode devices [2]. Several waveform generators have been proposed using current-mode devices; these waveform generator circuits offer several advantages over voltage-mode waveform generators. The circuits that are given in [3–14] are designed with Voltage Differencing Buffered/Inverted Amplifier (VDIBA), Multiple Output Current Through Transconductance Amplifiers (MO-CTTA), Controlled Gain Current and Differential Voltage Amplifier

(CG-CDVA), Differential Voltage Current Conveyors (DVCC), and Operational Transconductance Amplifier (OTA). These square-wave generators require external voltage or current biasing to produce the square waveform. Current Feedback Operational Amplifier (CFOA) based waveform generator was introduced in [15]. However, this waveform generator requires more passive components and two active components. A single CFOA based waveform generator was proposed in [16]. The configuration of the circuit is simple with a few passive components. However, the oscillation frequencies are limited to few kHz. Second generation Current Conveyor (CCII+) based waveform generators were proposed in the literature [17–21]. These waveform generators provide some advantages, like higher slew rate and wider bandwidth. However, some of these waveform generators require more than one active device and more passive components. Square-wave generators with single CCII+ were proposed in [20]. These waveform generators have the advantage of less power consumption. However, the oscillation frequencies of these circuits are limited to only few kHz. The square-wave generator using three operational transconductance amplifier (OTA) and three passive components was proposed in [22]. The advantage of this waveform generator would be that it can control the amplitude and frequency independently by changing the resistance or changing the biasing current. However, this waveform generator consumes more power and the use of three OTAs requires more chip area. Table 1 shows the comparison of active devices.

Table 1. Performance comparison of active devices.

Parameters	Op-amp	CFOA	CCII+	CDBA	OTA	OTRA
Power Supply	0.8 V	1.8 V	1.8 V	1.5 V	0.5 V	1.8 V
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Power Dissipation	190 µW	–	206 µW	194 µW	215 µW	210 µW
Open Loop Gain	66 dB	75 dB	78 dB	85 dB	52 dB	96 dB
Gain Band Width Product	3.4 MHz	23 MHz	–	100 MHz	7.5 MHz	152 MHz

Recently, an active current-mode device, called an operational transresistance amplifier (OTRA), has come to limelight with the introduction of several high performances CMOS OTRA realizations. Several waveform generators using an operational transresistance amplifier (OTRA) were reported earlier in the literature [23–42]. Square-waveform generator using single OTRA and a few passive components was proposed in [28]. Figure 1 shows this proposed circuit. The architecture of the circuit is simpler than the voltage-mode waveform generators. This circuit generates oscillations up to a few MHz. However, this circuit exhibits non-linear variation of time period with respect to the resistance R_2.

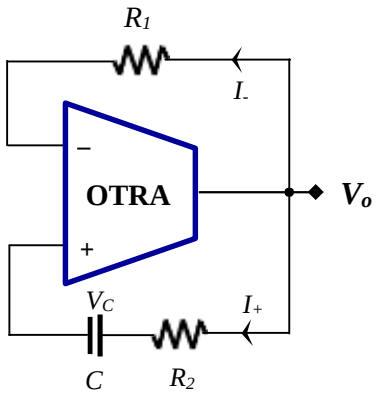


Figure 1. Conventional Operational Trans-resistance Amplifier (OTRA) based square-wave generator [28].

In this paper, two new square-wave generators based on single OTRA are presented. The proposed circuits are able to overcome the non-linear variation of the time period with respect to the passive components. The remaining sections of the paper are designed, as follows. In Section 2, the function of the OTRA is introduced first and then the operation of the proposed configurations is described along with the non-idealities. Section 3 presents simulated and experimental results. Finally, the conclusion is drawn in Section 4.

2. Circuit Description and Operation

The OTRA is a three terminal current-mode analog device with two low-impedance input terminals and one low-impedance output terminal [27,28]. The input terminals of the OTRA are virtually grounded, this leads to the circuits that are insensitive to the parasitic capacitances. Figure 2 shows the circuit symbol of the OTRA. The input and output terminal relations of an OTRA can be characterized by the following matrix. For ideal operation, the transresistance gain R_m approaches infinity, forcing the input currents to be equal.

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \quad (1)$$

$$V_+ = V_- = 0 \text{ and } V_o = R_m(I_+ - I_-) \quad (2)$$

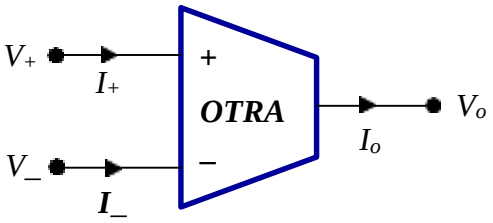


Figure 2. OTRA symbol.

Proposed Circuit-1

Figure 3 shows the first proposed square-wave generator. This square-wave generator consists of one active element (OTRA), one resistor R_1, one capacitor C, and two depletion mode NMOS transistors. The two NMOS transistors M_1 and M_2 are operated in the triode region and they act as a linear resistor.

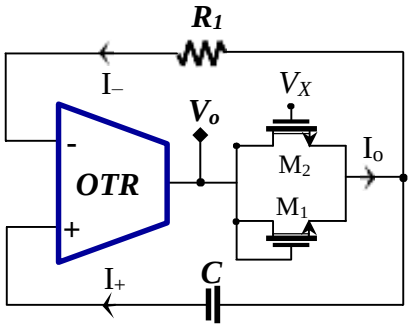


Figure 3. The first proposed current-mode square-wave generator configuration.

Equation (3) depicts the equivalent amount of resistance R_2 realized from the parallel combination of NMOS transistors as shown in Figure 4.

$$R_2 = \frac{1}{\mu_n C_{ox}(W/L)(V_X - 2V_T)} \quad (3)$$

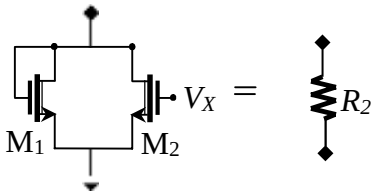


Figure 4. Resistor realization using two NMOS transistors [43].

This circuit generates a square-wave with almost equal and fixed on-duty and off-duty cycles, i.e., 50% duty cycles. Figure 5 shows the corresponding output waveform of the first proposed circuit. From Figure 5, it could be construed that the output square-wave (V_o) has two saturation levels V_{sat}^{+} and V_{sat}^{-}. Let us assume that V_o is at any one of these two saturation levels. If V_o changes its state from $V_{s}^{-}{}_{at}$ to V_{sat}^{+}, it implies that the current at the non-inverting terminal I_+ becomes more than the current at the inverting terminal I_- of the OTRA. At this moment, the voltage V_C of the capacitor C begins to increase from the lower threshold value V_{TL} to the final value V_{sat}^{+}. From Figure 3, the current I_o at the output terminal and the current I_- at the inverting input terminal of the OTRA can be written, as

$$I_o = \frac{V_o - V_C}{R_2} \tag{4}$$

$$I = \frac{V_C}{R_1} \tag{5}$$

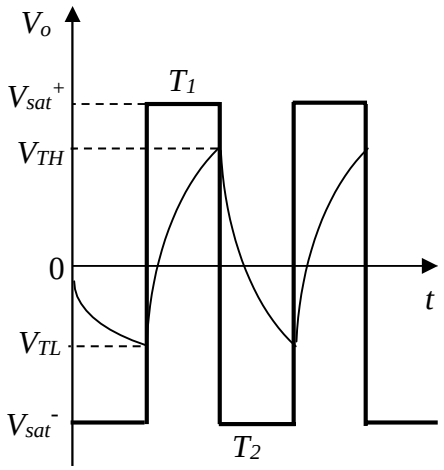


Figure 5. Output waveform of the proposed square-wave generators.

Subsequently, the non-inverting input terminal current I_+ can be expressed as

$$I_+ = \frac{V_o - V_C}{R_2} - \frac{V_C}{R_1} \tag{6}$$

From the terminal relations presented in Equation (1), V_o changes its state when the non-inverting terminal current is equal to the inverting terminal current $I_+ = I_-$. The capacitor voltage can be derived from Equations (5) and (6) by putting $I_+ = I_-$.

$$\therefore V_C = (R_1/2R_2 + R_1)V_o \tag{7}$$

The capacitor voltage changes between V_{TH} and V_{TL}. Subsequently, V_{TH} and V_{TL} can be derived from Equation (7) by substituting threshold and saturation values

$$V_{TH} = (R_1/2R_2 + R_1)V_{sat}^{+} \tag{8}$$

$$V_{TL} = (R_1/2R_2 + R_1)V_{sat}^- \tag{9}$$

The time evolution equation for the capacitor voltage V_C, when it starts to increase from V_{TL} towards its final value V_{sat}^+ can be expressed as

$$V_C(t) = (V_{TL} - V_{sat}{}^+)e^{\frac{-t}{R_2C}} + V_{sat}^+ \tag{10}$$

Time period T_1 can be derived by making $V_C(t) = V_{TH}$

$$T_1 = R_2C\ln(V_{TL} - V_{sat}^+)/(V_{TH} - V_{sat}^+) \tag{11}$$

By substituting V_{TH} and V_{TL} values from Equations (8) and (9)

$$T_1 = R_2C\ln\frac{(R_1/2R_2 + R_1)V_{sat}^- - V^+}{\cancel{(R_1/2R_2 + R_1)V_{sat}^+ - V_{sat}^+}} \tag{12}$$

From the output waveform, it can be written as

$$V_{sat}^+ = -V_s{}^-{}_{at} \tag{13}$$

$$T_1 = R_2C\ln\frac{(-R_1/2R_2 + R_1) - 1}{(R_1/2R_2 + R_1) - 1} \tag{14}$$

$$\therefore T_1 = R_2C\ln(1 + (R_1/R_2)) \tag{15}$$

The above Equation (15) is meant for on-duty cycle (T_{ON}). At the end of the on-duty cycle, the capacitor voltage V_C is charged up to the upper threshold voltage V_{TH}, instead of V_{sat}^+. At this point of time, the current at the non-inverting terminal I_+ becomes less than the current at the inverting terminal I_- of the OTRA. Subsequently, the output changes its state from the upper saturation level V_{sat}^+ to the lower saturation level $V_s{}^-{}_{at}$ and the capacitor starts discharging. When the voltage across capacitor C starts to decrease from V_{TH}, it can be expressed, as

$$V_C(t) = (V_{TH} - V_{sat}^-)e^{\frac{-t}{R_2C}} + V_{sat} \tag{16}$$

Time period T_2 can be derived by setting $V_C(t) = V_{TL}$

$$T_2 = R_2C\ln(V_{TH} - V_{s\,at}^-/V_{TL} - V_{s\,at}^-) \tag{17}$$

By substituting V_{TH} and V_{TL} values in the above Equation (16) and following the same demonstration as the on-duty cycle T_1, we obtain:

$$T_2 = R_2C\ln(1 + (R_1/R_2)) \tag{18}$$

The above Equation (18) is for off-duty cycle (T_{OFF}). The final time period (T) of the waveform is the sum of the T_1 and T_2 cycles.

$$T = T_{ON} + T_{OFF} = T_1 + T_2$$

$$T = 2R_2C\ln(1 + (R_1/R_2)) \tag{19}$$

For fixed duty cycles, the R_1, R_2, and C values will be obtained from the above Equation (19) for a required time period T. The required value of the resistor R_2 is calculated from (3) by adjusting the voltage V_X.

Proposed Circuit-2

The second proposed circuit that is shown in Figure 6 is designed to vary both the duty cycles independently with the help of resistors R_{11} and R_{12}. The voltage drops across these resistors used to control the operation of the diodes D_1 and D_2. The capacitor C starts charging towards V_{sat}^{+} when non-inverting terminal current is more than the inverting terminal current. This makes diode D_1 becomes forward bias and D_2 reverse bias. The diode D_1 and resistor R_{11} controls the amount of current at the inverting input terminal. Consequently, the on-duty cycle is more as compared to the off-duty cycle. Similarly, the diode D_2 becomes forward bias and D_1 reverse bias and capacitor starts discharging towards V_{sat}^{+} The resistor R_{12} and diode D_2 controls the inverting input terminal current. Due to this, the off-duty cycle is more when compared to the on-duty cycle.

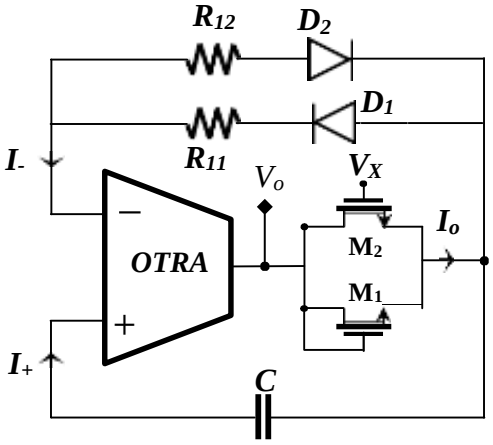


Figure 6. The second proposed square-wave generator configuration.

When considering ideal diodes (zero voltage drop), capacitor threshold voltages can be described by the following equations:

$$V_{TH} = (R_{12}/2R_2 + R_{12})V_{sat}^{+} \quad (20)$$

$$V_{TL} = (R_{11}/2R_2 + R_{11})V_{s\,at}^{-} \quad (21)$$

Time period T_1 (T_{ON}) can be obtained from Equations (20) and (21), while following the same demonstration reported in Section 2.1 for the proposed circuit-1

$$T_1 = R_2C\ln(V_{TL} - V_{sat}^{+}\ /V_{TH} - V_{sat}^{+}) \quad (22)$$

$$(R_{11}/2R_2 + R_{11})V_{s\,at}^{-} - V_{sat}^{+}\ .$$

$$T_{ON} = T_1 = R_2C\ln \quad (23)$$

$$^{12}/2R^{2} + R^{12})V^{+sat} - V^{+sat}$$

$$T_{ON} = R_2C\ln(1 + (R_{11}/R_2)) \quad (24)$$

Similarly for T_{OFF}

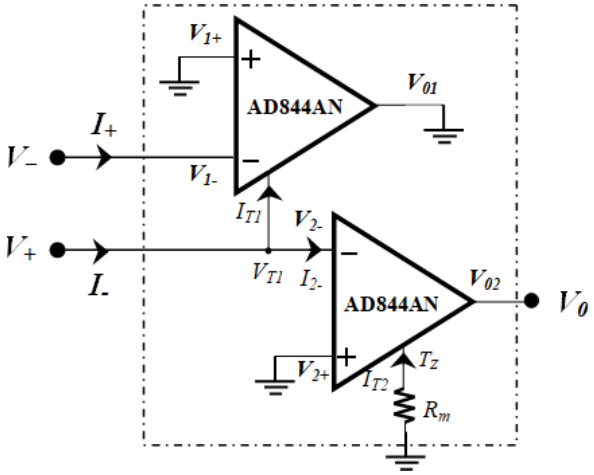
$$T_{OFF} = R_2C\ln(1 + (R_{12}/R_2)) \quad (25)$$

The total time period (T) for the proposed square-wave generator in Figure 6 can be expressed as $T = T_{ON} + T_{OFF}$

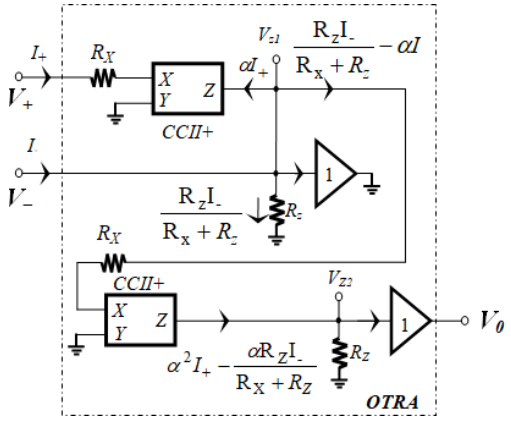
$$T = R_2C\ln((1 + (R_{11}/R_2)(1 + (R_{12}/R_2)) \quad (26)$$

Non-Ideal Analysis

An equivalent circuit model of the OTRA built with two current feedback amplifiers (CFAs) is shown in Figure 7a to consider the non-ideal and parasitic effects on the proposed circuits.



(a) OTRA implementation with two AD844AN.



(b) Non-ideal model of the adopted OTRA.

Figure 7. OTRA Equivalent Model [25–31].

A practical CFA (AD844AN IC) can be modeled as a positive second-generation current conveyor (CCII+) cascading a voltage buffer with finite parasitic resistances and non-zero current tracking errors. Figure 7a reveals a more detailed circuit model of the OTRA that is given in Figure 7b. Where R_X and R_Z are the parasitic resistances and α represents the current tracking error factor from the terminal T_Z with respect to the inverting terminal. The standard values of R_X, R_Z, and α are given in AD844AN datasheet are α = 0.98, R_X = 50 Ω, and R_Z = 3 MΩ. Figure 7a indicates the resultant expressions of the related currents. The voltage tracking error effect between the CCII+ input terminals are skipped (eliminated) in the circuit model, because of the non-inverting terminal for each CCII+ being connected to ground.

Non-Ideal Analysis of Proposed Circuit-1

For the proposed circuits, the non-ideal analysis gives the following equations

$$V_{TH} = (\alpha R_1/(\alpha R_1 + (R_2R_Z/R_X + R_Z) + R_2\alpha))V_{sat}^{+} \quad (27)$$

$$V_{TL} = (\alpha R_1/(\alpha R_1 + (R_2R_Z/R_X + R_Z) + R_2\alpha))V_{sat}^{-} \quad (28)$$

Substituting these higher and lower threshold voltages into Equations (11) and (17), the non-ideal time period of the proposed circuit in Figure 3 can be expressed, as

$$T = 2R_2C\ln(1 + (2\alpha R_1/(R_2R_Z/R_X + R_Z) + R_2\alpha) \quad (29)$$

Non-Ideal Analysis of Proposed Circuit-2

The non-ideal equation for the second proposed circuit in Figure 6 is given in Equation (32)

$$V_{TH} = (\alpha R_{12}/(\alpha R_{12} + (R_2R_Z/R_X + R_Z) + R_2\alpha))V_{sat}^{+} \quad (30)$$

$$V_{TL} = (\alpha R_{11}/(\alpha R_{11} + (R_2R_Z/R_X + R_Z) + R_2\alpha))V_{s\,at}^{-} \quad (31)$$

$$T = R_2C\ln((1 + \frac{2\alpha R_{11}}{(R_2R_Z/(R_X + R_Z)) + R_2\alpha})(1 + \frac{2\alpha R_{12}}{(R_2R_Z/(R_X + R_Z)) + R_2\alpha})) \quad (32)$$

It can be easily verified that Equations (29) and (32) reduces to Equations (19) and (26), as expected, for ideal OTRA when $\alpha \approx 1$ and $R_X \approx 0$.

3. Simulation and Experimental Results

The proposed circuits were simulated using SPICE CMOS model parameters with a supply voltage of ±1.8 V. Figure 8 provides the CMOS realization of the OTRA. Table 2 depicts the aspect ratios of the transistors, biasing voltages, and biasing currents. Figure 9 provides the simulated output results of the proposed circuits.

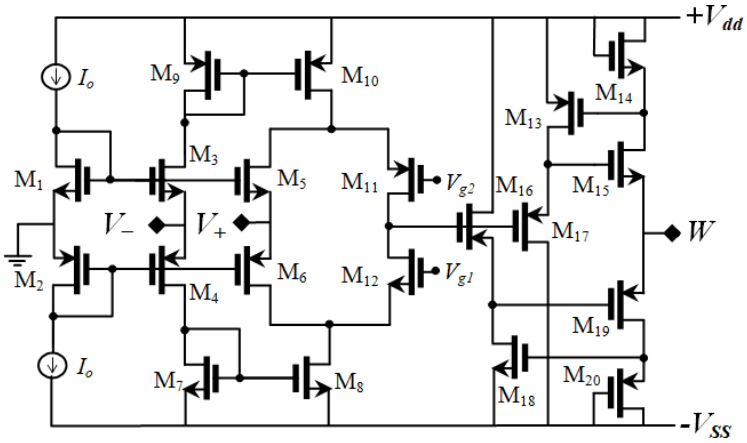
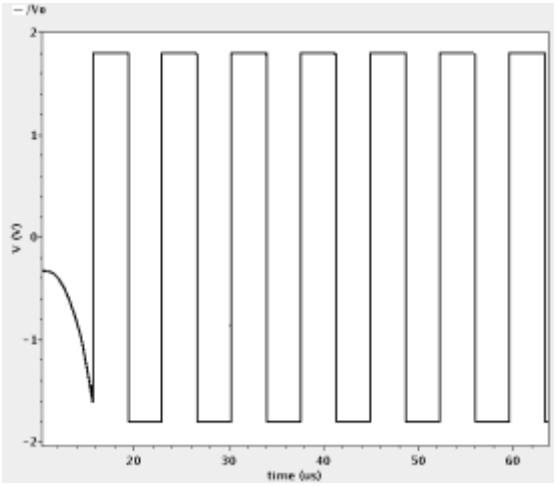


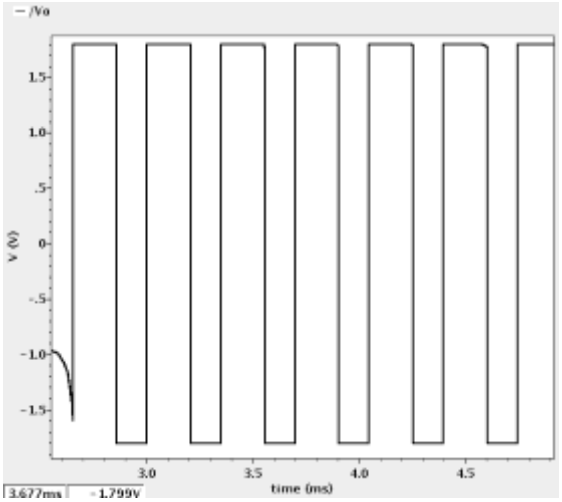
Figure 8. The device level circuit diagram of the OTRA [31].

Table 2. Aspect ratios of the circuit shown in Figure 8.

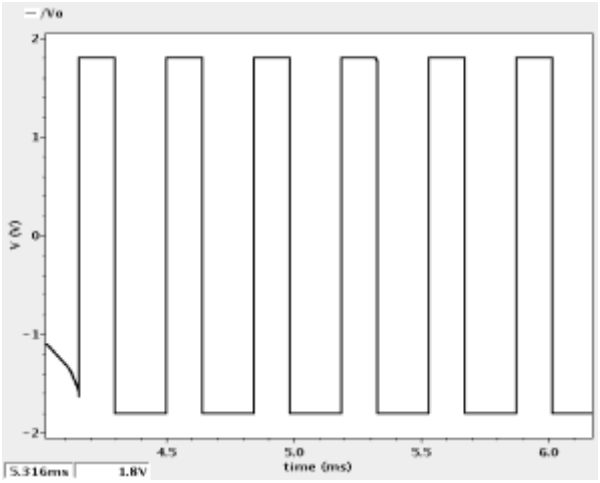
Table	W (μm)	L (nm)
M_1-M_6	4	180
M_7-M_{10}	6	180
M_{11}-M_{12}	20	180
M_{14}, M_{20}	2	180
M_{13}, M_{18}	12	180
M_{15}	12	180
M_{16}, M_{19}	4	180
M_{17}	3.3	180
$V_{g1} = V_{g2}$ = 0.8 V and I_0 = 40 μA		



(a) Output waveform of the proposed circuit-1 (T_{ON} =T_{OFF}).



(b) Output waveform of the proposed circuit-2 (T_{ON}>T_{OFF}).



(c) Output waveform of the proposed circuit-2 (T_{ON}<T_{OFF}).

Figure 9. Output waveforms of the proposed square-wave generators.

For generating the square-wave of the first proposed circuit in Figure 3, the required time period is chosen first. Subsequently, the ratio of R_1/R_2 is taken care of and the value of capacitor C is arbitrarily

determined from Equation (19). The voltage V_X is adjusted to realize the desired value of resistance R_2 from (3). However, with this circuit the on-duty and off-duty cycles are fixed. The first proposed circuit was designed with the following passive components R_1 = 15 kΩ, R_2 = 1.5 kΩ (W = 5μm, L = 180 nm, V_X = 80 mV), and C = 1 nF to generate the square waveform. Figure 9a shows the simulated output waveform of the proposed circuit in Figure 3 with a time period of 7.56 μs, which is close to the theoretical time period of 7.19 μs.

For the second proposed circuit in Figure 6, the values of resistors R_{11} = R_{12}, equivalent resistance R_2 and capacitor C, are derived from the above process as stated in fixed duty cycles. Then the resistors R_{11} and R_{12} are tuned independently in order to set the required on-duty and off-duty cycles. If resistor R_{11} is chosen to be greater than the resistor R_{12}, then the on-duty cycle is more than the off-duty cycle. These values will be (R_{12} > R_{11}) reversed to set the off-duty cycle more than the on-duty cycle. The passive components R_2 =1.5 kΩ (W = 5μm, L = 180 nm, V_X = 80 mV), R_{11} = 1.5 kΩ, R_{12} = 5 kΩ, and C = 0.1μF were used to design the second proposed circuit in Figure 6. Figure 9b,c provide the corresponding simulated output waveforms for the second proposed circuit. From Figure 9b,c, the simulated time period is 0.36 ms, which is close to the theoretical time period of 0.32 ms.

AD844AN is adopted to construct the proposed circuits on a laboratory breadboard in order to verify the theoretical study. The commercial IC AD844AN with current feedback architecture (configuration) is used to implement the OTRA, as shown in Figure 7a [27,28]. Therefore, the behavior of the OTRA is obtained with the schematic shown in Figure 7a. For the proposed circuit in Figure 3, the required time period is chosen first. Subsequently, suitable values of passive components (R_1, R_2, and C) are derived from Equation (19). In all measurements, the passive component R_2 value is the same as the resistance R_2 value calculated from Equation (3). For higher sensitivity of the time period with respect to the resistor, the resistor R_2 is chosen to be less than 2 kΩ. The experimental output waveform of the proposed circuit-1 is given in Figure 10 with a time period of 7 μs.

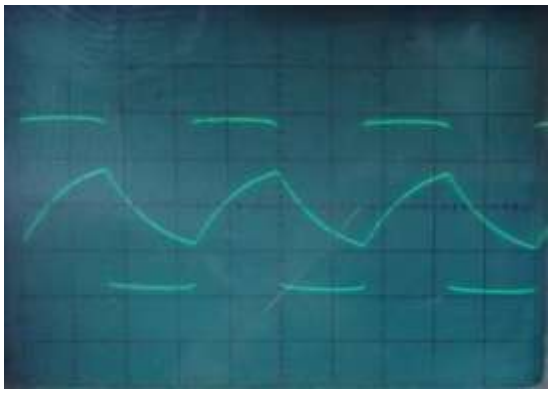
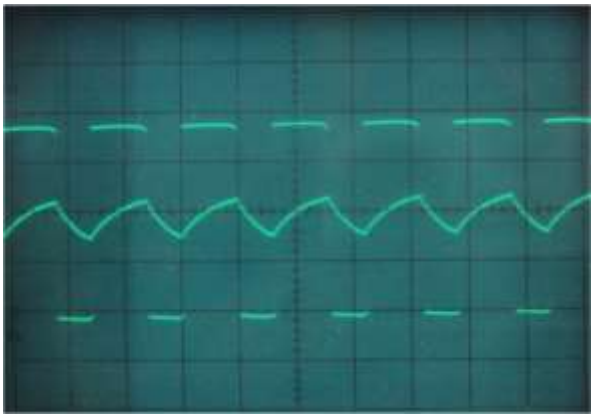
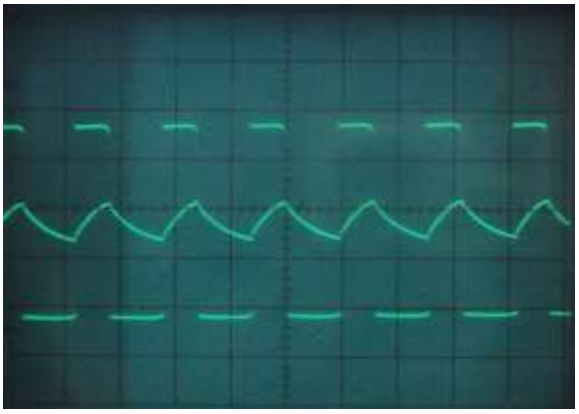


Figure 10. Output waveform with almost equal and fixed duty cycles (T_{ON} = T_{OFF}). Scale: X-axis 2 μs/div and Y-axis 1 V/div.

Similarly, in the case of the second proposed circuit, the suitable passive component values will be obtained from Equation (26) to a chosen time period. If the required time period is 0.32 ms with 60% on-duty and 40% off-duty cycles then the capacitor C is slightly increased to set the required time period. The resistor R_{11} and R_{12} values will be reversed to set the 40% on-duty and 60% off-duty cycles. The output waveforms for the second proposed circuit are given in Figure 11a,b with a time period of 0.31 ms.



(a) Output waveform with variable on-duty cycle (T_{ON}>T_{OFF}). Scale: X-axis 0.2 ms/div and Y-axis 1 V/div.



(b) Output waveform of with variable off-duty cycle (T_{ON}<T_{OFF}). Scale: X-axis 0.2 ms/div and Y-axis 1 V/div.

Figure 11. Experimental output waveforms of the second proposed circuits.

Several experiments were performed on the laboratory bread board to test the tunability of the proposed circuits against the passive components R_1, R_2, and C. The results are presented in Figures 12–15 for the proposed circuit configuration in Figure 3. The supply voltage of ±6 V was used for all measurements on tunability.

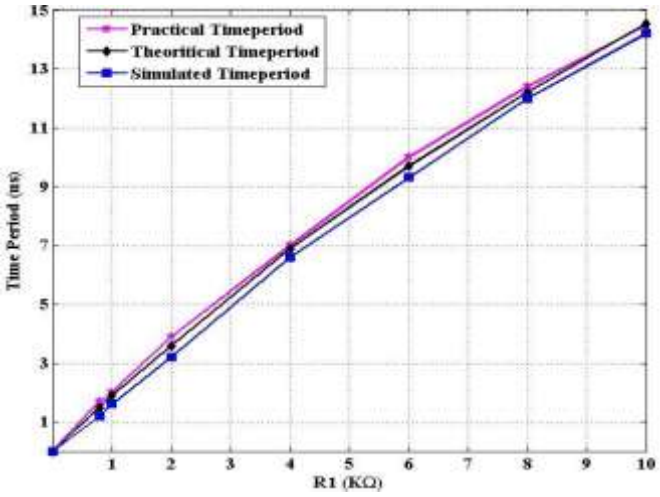


Figure 12. Variation of time period against resistor R_1.

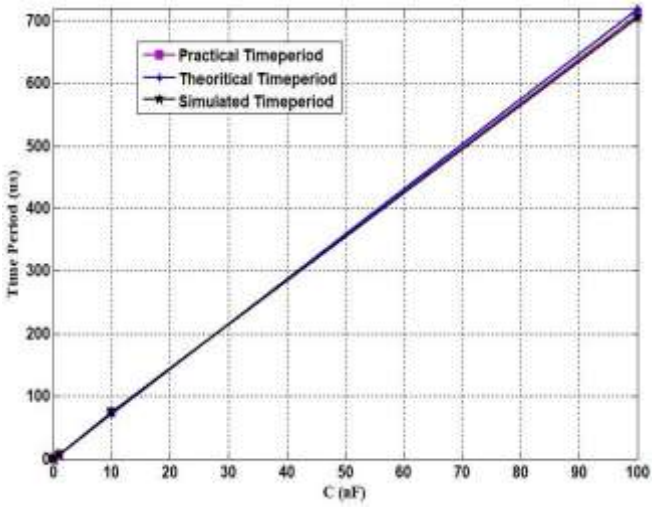


Figure 13. Tunability against capacitor *C*.

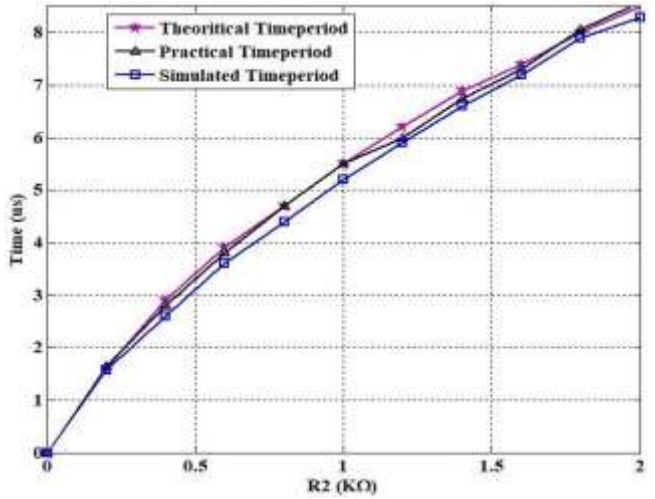


Figure 14. Tunability against resistor R_2.

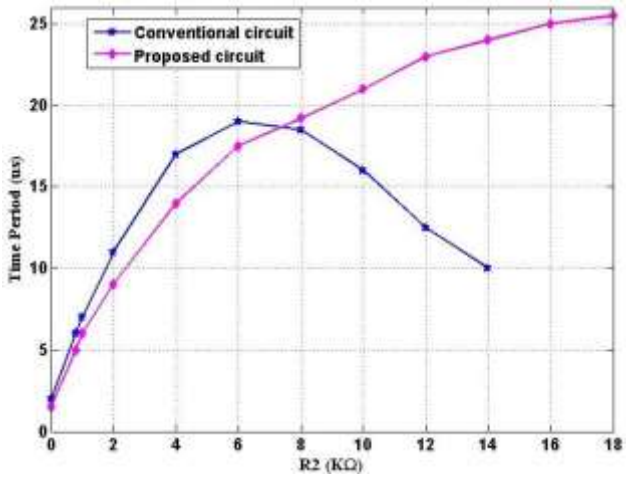


Figure 15. Time period variation between conventional and proposed circuits against R_2.

Figures 12–14 denote the time period variation against the passive components R_1, R_2, and C. For the tunability of resistor R_1, the selected passive component values are R_2 = 12 kΩ and C = 1 nF and R_1 was varied from 800 Ω to 10 kΩ.

A linear like variation of time period was exhibited by the circuit and it is presented in the form of plot in Figure 12. Similarly, for the capacitor C, the selected parameter values are resistors R_1 = 15 kΩ and R_2 = 1.5 kΩ. The capacitor C was varied from 0.1 nF to 100 nF. Figure 13 plots the practical and theoretical time period variation against the capacitor C. Likewise, for the resistor R_2, the circuit was built with resistor R_1 = 15 kΩ, capacitor C = 1 nF and R_2 was varied from 200 Ω to 3 kΩ.

From Figures 12–14, the variation of the time period with respect to the passive components is linear. Figure 1 shows the OTRA based square-wave generator proposed in [28]. For generating the square-wave in the circuit shown in Figure 1, it is necessary to maintain the resistor R_2 value less than the resistor R_1 and as it will not generate the waveform when $R_1 < R_2$. The proposed circuits in Figures 3 and 6 will generate the waveform independent of the resistor values and exhibit more linear curve than the conventional circuit in Figure 1. Figure 15 shows the comparison between conventional OTRA square-wave generator circuit [28] and proposed square-wave generator circuit in Figure 3. For the plot in Figure 15 the parameters values are R_1 = 15 kΩ and C = 1 nF, and R_2 was varied from 200 Ω to 18 kΩ. From Figure 15, it can be construed that the proposed circuit exhibits more linear curve than the conventional circuit. The proposed circuits can generate the oscillations up to 1.2 MHz. A detailed tally of the proposed circuit with the other square-wave generators in the literature are presented in Table 3 in order to highlight the advantage of the proposed circuit in Figure 3. Form this comparison table, the proposed circuit outperforms with most of the listed square wave generators. The square waveform generators reported in [12,15] generates a high frequency of oscillations when compared with the proposed circuits. With two active components along with passive component consume a high amount power and occupy large silicon area. The square wave generator that is given in [44] requires two passive components (one resistor and one capacitor) and one passive component to produce high frequency oscillations. However, the active device Dual-X Current Conveyor Transconductance Amplifier (DXCCTA) is very bulky with eight input terminals and one output terminal. The total number of transistors to construct the DXCCTA is also large. A greater number of transistors and input terminals increase the silicon area and power consumption.

Table 3. Comparison of the proposed circuit in Figure 3 with the conventional circuits in the literature.

References	No. of Active Components	No. of Passive Components	Total Components	Maximum Frequency Range	Supply Voltage
[9]	2 DVCC	4 (1 C & 3 R)	6	860 kHz	±10 V
[12]	2 VDIBA	3 (1 C & 2 R)	5	2.8 MHz	±5 V
[15]	2 CFOA	5 (1 C & 4 R)	7	15 MHz, [1]S	±5 V
[16]	1 CFOA	4 (1 C & 3 R)	5	71 kHz	–
[17]	3 CCII+	7 (1 C & 6 R)	10	574 kHz	±6 V
[19]	2 CCII+	4 (1 C & 3 R)	6	260 kHz	±5 to ±15 V
[20]	2 CCII+	6 (1 C & 5 R)	8	737 kHz	±15 V
[21]	1 CCII+	4 (1 C & 3 R)	5	2 kHz	1.5 V, [3]I.S.
[22]	3 OTA	3 (1 C & 2 R)	6	16 kHz	±5 V
[44]	1 CDTA	2 (1 C & 1 R)	4	600 kHz	±2.5 V, [1]S ±9 V, [2]H
[45]	1DXCCTA	2 (1 C & 1 R)	3	20.6 MHz	±1.25 V, [1]S
[28]	1 OTRA	3 (1 C & 2 R)	4	1.0 MHz	±15 V
Proposed Figure 3 circuit	1 OTRA	2 (1 C & 1 R)	3+2 NMOS Transistors	1.5 MHz, [1]S 1.2 MHz,[2]H	±1.8 V, [1]S ±6 V, [2]H

[1]S = Simulation, [2]H = Hardware Implementation, [3]I.S. = Integrate Solution.

4. Conclusions

Two new square-wave generators are suggested in this study. The suggested circuits are less complicated than voltage-mode (op-amp based) waveform generators since they only utilise one OTRA and a few passive components. These topologies have the notable feature of being implemented with commercially available ICs AD 844 AN. The time period with regard to the passive component varies linearly in the suggested circuits. Also, by modifying the voltage, the suggested circuits' time period can be electronically tweaked (VX).The results exhibited by such topologies congruent with the simulated as well as the theoretical values. The proposed circuits can generate oscillations up to 1.2 MHz (experimental). These circuits can be expected to find wider applications in many applied electronics, communications, instrumentation, and signal processing applications.

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